NanoSpice X

PRIMARIUS

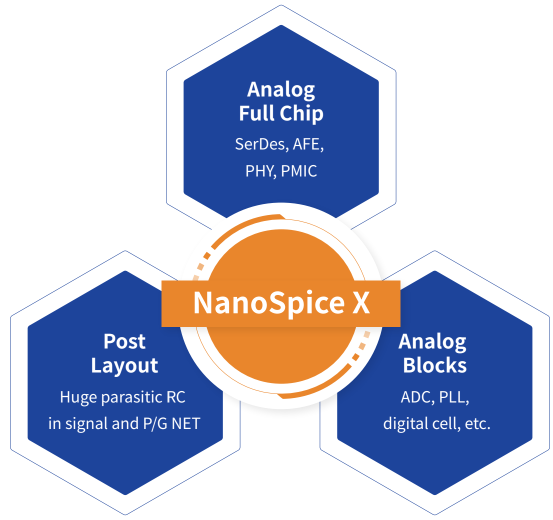
Circuit Driven SPICE Simulator

Introduction

As a high-precision and high-capacity parallel SPICE simulator, NanoSpice X is designed to tackle the most challenging simulation tasks for accurate block level circuits, complicated analog full chip designs and large post-layout analog circuits with huge parasitic RC on Power and Ground Net.

With superior parallelization technologies, adaptive SPICE Solver, efficient Matrix solving, post-layout circuit topology optimization and significantly enhanced RC reduction capacities, NanoSpice X empowers simulations of remarkable scale, accommodating up to 100 million circuit elements while preserving SPICE-level accuracy.

Moreover, NanoSpice X features an innovative parallelization license model that offers a cost-effective choice for designers.



Key Advantages

- Faster Speed
  - 2X to 10X+ faster than other solutions with the same precision
  - Efficiently handle the time-consuming part in analog full chip with digital blocks
  - Faster simulation runtime in trannoise analysis
- More Comprehensive
  Mature digital-centric and analog-centric flows
- Higher Accuracy
  True SPICE engine following the highest industry standard
- Larger Capacity
  Larger capacity than other SPICE, especially for post-layout
- Compatibility
  Standard input/output formats and fully compatible SPICE features
- Expansion
  From analog blocks to analog full chip

Application Examples

Type	Circuit Size	REF	NanoSpice X	Speedup
SerDes	MOS: 459K; R: 11.03M; C: 10.5M	> 1440h	187h	8X
ADC	MOS: 171K; R: 4.9M; C: 12.9M	132h	31h	4.3X
PLL	MOS: 57.8K; R: 475K; C: 167K	160h	79h	2X
VCO	MOS: 381K; R: 1.04M; C: 25K	72.4h	37.1h	2X
PMU	MOS: 14.7K; R: 1.25M; C: 1.85M	62h	26h	2.4X

Specifications

- Supports mixed-signal co-simulation
- Supports 3D-IC and multi-technology simulation (MTS)
- Supports Comprehensive Circuit Check (CCK) and Safe Operation Area (SOA) simulation
- Supports statistical analysis including PVT, Monte Carlo,and High Sigma
- Supports public cloud platform, hybrid cloud and private cloud
- Supports S-parameter, Transmission line (W-element, T-element)
- Supports IBIS model
- Supports SPEF, DSPF, DPF back-annotation
- Full SPICE analysis features
  - OP, DC, AC, Noise, Transient, Trannoise, FFT, Sweep, Alter, Bisection Stability, Pole-Zero, MonteCarlo, DC Match, AC Match
- Supports standard output formats for data analysis:
  - FSDB,PSFASCII, PSFBIN, SPICEASCII, ASCII, etc.
- Supports HSPICE and Spectre netlist formats
- Supports all public domain models, user-defined models
  - MOSFET: BSIM3, BSIM4, BSIM-BULK, BSIM-IMG, BSIM-CMG BSIM-SOI, LETI-UTSOI, PSP, HiSIM2, HiSIM_HV, EKV3
  - BJT: MAXTRAM, VBIC, HICUM
  - TFT: a-Si TFT, poly-Si TFT
  - Diode: JUNCAP, JUNCAP200, DIODE_CMC
  - Varactor: MOSVAR
  - Resistor: R2_CMC, R3_CMC
  - HEMT: ASM-HEMT
  - JFET
  - MESFET
- Supports TMI & Custom PMI
- Supports Verilog-A (LRM2.4) and behavioral sources
- Supports VEC and VCD stimulus files

Applications

- Analog full-chip simulation (Serdes, PLL, PHY, etc.)
- Mixed-signal co-simulation
- Full customized digital circuit simulation
- Standard Cell characterization and verification