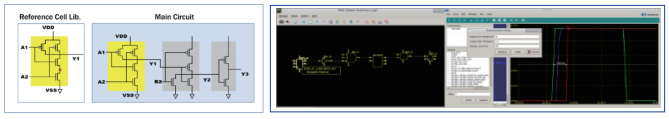
TRASTA

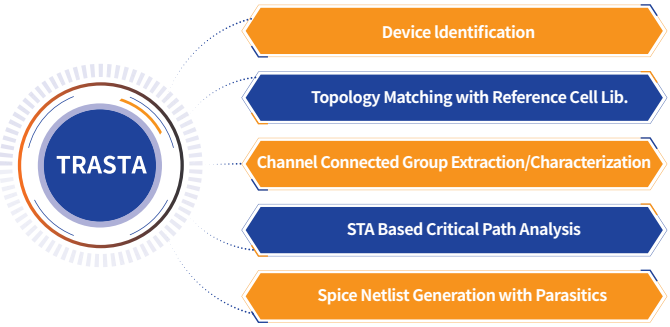
PRIMARIUS

Gate-TR Mixed-level Timing Analysis Solution

Introduction

Transistor level circuit simulation is the essential step of the integrated circuit (IC) design. However, it is generally impractical to simulate the entire SoC at the transistor level. Designers need to identify the critical path and should be able to analyze the selected critical path with the highest accuracy within the limited design time. TRASTA automatically identifies the critical path and enables designers to analyze the critical path with the highest precision. TRASTA automatically identifies the unique devices of the design and generates the gate level circuit with topology matching and channel connected extraction techniques. The timing characteristics of extracted gate-level cells are automatically characterized and it is used in Static Timing Analysis (STA) step. TRASTA provides a built-in STA engine and SPICE netlist generation capability with back-annotated parasitics.





Key Advantages

- Efficient critical path tracing at the full-chip level
- Automatic critical path extraction with parasitics
- On the fly custom cell characterization
- Unified environment for STA and dynamic simulation

Applications

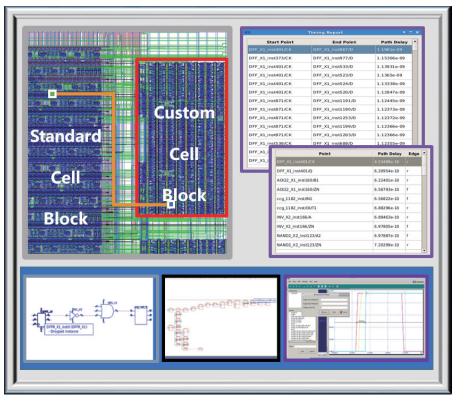
- Custom cell characterization
- Timing analysis of the mixed design
- Re-characterization of standard cell
- Timing analysis of CPU datapaths/Digital IPs

Specifications

- Automatic gate abstraction
  - MCCG (Multiple CCG) cell extraction
  - Custom cell name/topology matching
  - CCG (Channel Connected Group) cell extraction
- Automatic custom / CCG cell characterization
  - Timing library generation for NLDM / CCS / ECSM
- Full chip static timing analysis
  - Gate-level static timing analysis
  - Linking custom design and standard cell design
- SPICE simulation interface
  - Critical path expanding with parasitics
  - Interactive cross-probing with the waveform viewer

Application Examples

Timing Analysis



Automatic False Path Detection